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10/609,119	06/27/2003	Holly G. Gates	INK-109	6703

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DAVID J COLE
E INK CORPORATION
733 CONCORD AVE
CAMBRIDGE, MA 02138-1002

EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,119	GATES, HOLLY G.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 33-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear why the addressing voltage is less than a voltage level of the voltage source at the end of the period of time since the resistive switch was turn on for a period of time, as recited in independent claim 33?

It is not clear what is a portion of one sub-cycle, as recited in claim 35?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 12, 16-17, 20-21, 23-26, 31-33, 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Proebsting (US Patent No. 5,952,948).

As to claim 1, Proebsting teaches a method for addressing a display medium (See Col. 1, Lines 5-9), the method comprising the steps of:

providing a plurality of voltage sources each having a different voltage level (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 3-24);

receiving a display signal indicating an addressing impulse to be applied to a pixel electrode (See Fig. 1, items 102, 104, 106, Col. 1, Lines 41-45);

selecting, responsive to the display signal, a portion of the plurality of voltage sources (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 25-29);and

connecting the selected voltage sources to a switch circuit that is connected to the pixel electrode (See Figs. 1-3, items 110, 112, Col. 2, Lines 29-33).

As to claim 2, Proebsting teaches the step of connecting the selected voltage sources comprises simultaneously connecting the selected voltage sources to the switch circuit (See Fig. 4, items 404, 406, N1, N2, Col. 4, Lines 10-21).

As to claim 3-4, 20 Proebsting teaches the step of connecting the selected voltage sources comprises sequentially connecting the selected voltage sources to the pixel unit and activating the switch circuit to connect the selected voltage sources to the pixel electrode (See Fig. 4, items 408, 410, N1, N2, OUT, Col. 4, Lines 22-34).

As to claim 5, 21, 32, 36 Proebsting teaches wherein the switch circuit comprises a transistor, and the step of activating the switch circuit comprises applying a selection voltage to a gate of the transistor (See Fig. 5A, items 406, 408, Col. 5, Lines 7-15).

As to claim 12, Proebsting teaches voltage levels have fixed voltage amplitude values (See Fig. 3, items 6,4 v, 6.2 v, ...).

As to claims 16, 26 Proebsting teaches storing data that identifies a present optical state of a portion of the display medium defined by the pixel electrode, and wherein the step of selecting the portion of the plurality of voltage sources comprises comparing a new optical state associated with the addressing impulse to the present optical state (see fig. 1, item 104, Col. 1, Lines 37-45).

As to claim 17, Proebsting teaches a method for addressing a display medium (See Col. 1, Lines 5-9), the method comprising the steps of:

providing a capacitive element to apply an addressing voltage to a portion of the display medium (See Fig. 1, item 112, Col. 1, Lines 57-60).

providing a voltage sources each having a voltage level greater than addressing voltage (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 3-24); and

charging the capacitive element with the voltage source until the capacitive element applies the addressing voltage (See Figs. 1-3, items 110, 112, Col. 2, Lines 29-33).

As to claim 23, Proebsting teaches capacitive element comprises a pixel electrode (See Fig. 1, item 112, Col. 1, Lines 57-60).

As to claim 24, Proebsting teaches an addressing structure for addressing a display medium (See Col. 1, Lines 5-9), the structure comprising:

a pixel electrode (See Fig. 1, item 112, Col. 1, Lines 57-59);

a switch circuit connected to the pixel electrode (See Fig. 1, item 110, Col. 1, Lines 57-59);

a plurality of voltage sources each having a different voltage level (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 3-24); and

a switch unit configured to connect a portion of the plurality of voltage sources to the switch circuit responsive to a display signal indicating an addressing impulse (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-3, item 204-8, Col. 2, Lines 29-33).

As to claim 25, Proebsting teaches a voltage selector that selects the portion of plurality of voltage sources (See Fig. 3, item 204-8, Col. 2, Lines 25-33).

As to claim 31, Proebsting teaches a display signal generator configured to generate the display signal (See Fig. 1, Item 100, Col. 1, Lines 38-41).

As to claim 33, as best understood by examiner, Proebsting teaches an addressing structure for addressing a display medium (See Col. 1, Lines 5-9), the structure comprising:

a voltage source (See Fig. 3, item 202-8, Col. 2, Lines 26-33);

a capacitive element to apply an voltage to a display medium defined by a pixel electrode (See Fig. 1, item 112, Col. 1, Lines 57-60)

a resistive switch configured to connect the voltage source to the capacitive element (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-3, item 204-8, Col. 2, Lines 29-33); and

an addressing voltage controller configured to turn the resistive switch on for a period of time to gradually charge the capacitive element until the capacitive element

applies an addressing voltage that is less than a voltage level of the voltage source at the end of the period of time (See Fig. 1, item 112, Col. 1, Lines 57-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-11, 13-15, 22, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting as applied to claims 1, 17, 24 in view of Kageyama et al. (Pub. No.: US 2002/0180679 A1).

As to claim 6, Proebsting does not disclose the display signal comprises a voltage magnitude number having digits that are associated with different ones of the plurality of voltage levels, and the step of selecting the portion of the plurality of voltage sources comprises selecting those of the plurality of voltage sources that are indicated for selection by the digits of the number.

Kageyama et al. teaches the display signal comprises a voltage magnitude number having digits that are associated with different ones of the plurality of voltage levels, and the step of selecting the portion of the plurality of voltage sources comprises selecting those of the plurality of voltage sources that are indicated for selection by the digits of the number (See Figs. 3A-3B, items 0-15, paragraphs 0061-0063).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kageyama et al. into Proebsting system in order to reduce a number of voltage (See paragraph 0027 in the Kageyama et al. reference).

As to claim 7, Kageyama et al. teaches wherein the voltage magnitude number is a binary number, and the step of selecting the portion of the plurality of voltage sources further comprises selecting those of the plurality of voltage sources that are indicated for selection by the digits of the binary number that have a value of 1 (See Figs. 3A-3B, items 0,1, paragraph 0064-0065).

As to claim 8, it is obvious that change of n-channel and p-channel transistors to opposite channels will allow to use the binary number that have a value of 0 (See paragraph 0061 in the Kageyama et al. reference).

As to claim 9, Kageyama et al. teaches each of the digits of the voltage magnitude number is associated with one of a plurality of sub-cycles of an addressing cycle, and the step of connecting the selected voltage sources comprises connecting each of the selected voltage sources during the associated sub-cycle (See Fig. 5, items S1-S4, paragraph 0068).

As to claim 10, Proebsting does not disclose the display signal indicates a sequence of addressing impulses associated with a sequence of addressing cycles of the display, and wherein the steps of selecting the portion of the plurality of voltage sources and connecting the selected voltage sources are repeated for each of the sequence of addressing impulses.

Kageyama et al. teaches the display signal indicates a sequence of addressing impulses associated with a sequence of addressing cycles of the display, and wherein the steps of selecting the portion of the plurality of voltage sources and connecting the selected voltage sources are repeated for each of the sequence of addressing impulses (See Fig. 5, items S1-S4, paragraph 0068).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kageyama et al. into Proebsting system in order to reduce a number of voltage (See paragraph 0027 in the Kageyama et al. reference).

As to claim 11, Proebsting does not disclose selecting none of the plurality of voltage sources.

Kageyama et al. teaches selecting none of the plurality of voltage sources Ises (See Fig. 6, items 0, V0, paragraph 0069).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kageyama et al. into Proebsting system in order to reduce a number of voltage (See paragraph 0027 in the Kageyama et al. reference).

As to claim 13, Proebsting does not disclose the display signal indicates a sequence of addressing impulses to be applied to a plurality of pixel electrodes during one addressing cycle of the display.

Kageyama et al. teaches the display signal indicates a sequence of addressing impulses to be applied to a plurality of pixel electrodes during one addressing cycle of the display (See Fig. 5, items S1-S4, paragraph 0068).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kageyama et al. into Proebsting system in order to reduce a number of voltage (See paragraph 0027 in the Kageyama et al. reference).

As to claims 14, 27-29 Kageyama et al. teaches the step of connecting the selected voltage sources to the switch circuit comprises connecting the selected voltage sources to a column electrode connected to a plurality of switch circuits that are each connected to a different one of the plurality of pixel electrodes (See Fig. 2, SL1-SI4, paragraphs 0067-0068).

As to claim 30, Kageyama et al. teaches aselection signal generator configured to apply selection signal to one of plurality of pixel electrodes when connecting the column electrode to the selected voltage sources associated with one of the plurality of pixel electrodes (See Fig. 2, items 23, 28, paragraph 0067).

As to claim 15, Kageyama et al. teaches the step of activating one of the plurality of switch circuits to connect the selected voltage sources to an associated one of the plurality of the pixel electrodes associated with the addressing impulses (See Fig. 2, SL1-SI4, paragraphs 0067-0068).

As to claim 22, Proebsting teaches selecting a capacitance of the capacitive element (See Fig. 1, item 112, Col. 1, Lines 57-60).

Proebsting does not disclose selecting a resistance of resistive circuit to control charging rate of the capacitive element.

Kageyama et al. teaches selecting a resistance of resistive circuit (See Fig. 2, items r, Rsw, paragraph 0059-0060).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kageyama et al. into Proebsting system in order to reduce a number of voltage (See paragraph 0027 in the Kageyama et al. reference).

4. Claim 18-19, 34-35, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting as applied to claim 17 above, and further in view of Reddy (US patent No. 6,175,355).

As to claims 18-19, Proebsting does not disclose charging the capacitive element comprises charging the capacitive element during a sub-cycle of a plurality of sub-cycles of an address cycle to apply the addressing voltage or portion of an addressing impulse to the display medium during subsequent sub-cycles of the address cycle.

Reddy teaches charging the capacitive element comprises charging the capacitive element during a sub-cycle (in the reference sub-frame) of a plurality of sub-cycles (in the reference sub-frame) of an address cycle (in the reference frame) to apply the addressing voltage or portion of an addressing impulse to the display medium during subsequent sub-cycles of the address cycle (See Fig. 5, items PS0-PS15, Col. 3, Lines 23-42).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Reddy into Proebsting system in order to modulate each pixel for forming a grey-scale image on the display (See Col. 1, Lines 6-10 in the Reddy reference).

As to claims 34-35, as best understood by examiner, Proebsting does not disclose wherein the period of time is associated with at least one sub-cycle or a portion of sub-cycle of a plurality of sub-cycles of an addressing cycle, and the addressing voltage controller is configured to select the at least one sub-cycle or a portion of sub-cycle in response to an addressing signal.

Reddy teaches charging the capacitive element comprises charging the capacitive element during a sub-cycle (in the reference sub-frame) of a plurality of sub-cycles (in the reference sub-frame) of an address cycle (in the reference frame) to apply the addressing voltage or portion of an addressing impulse to the display medium during subsequent sub-cycles of the address cycle (See Fig. 5, items PS0-PS15, Col. 3, Lines 23-42).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Reddy into Proebsting system in order to modulate each pixel for forming a grey-scale image on the display (See Col. 1, Lines 6-10 in the Reddy reference).

As to claim 37, Proebsting does not disclose the addressing voltage controller comprises a pulse width modulator.

Reddy teaches the addressing voltage controller comprises a pulse width modulator (See Col. 2, Lines 1-10).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Reddy into Proebsting system in order to modulate

each pixel for forming a grey-scale image on the display (See Col. 1, Lines 6-10 in the Reddy reference).

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
08.31.05

VIJAY SHANKAR
PRIMARY EXAMINER